Rapid-thermal-annealing effect on lateral charge loss in metal–oxide–semiconductor capacitors with Ge nanocrystals

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The rapid-thermal-annealing effect on lateral charge loss in metal–oxide–semiconductor capacitors with Ge nanocrystals is investigated by means of capacitance-voltage (C–V) and capacitance decay measurements. The C–V curves show the hysteresis indicating the charge storage effect in Ge nanocrystals. The hysteresis width shows strong annealing temperature dependence and shows the maximum at 700 °C meaning the maximum nanocrystal density. Capacitance decay experiment at flat-band voltage shows that the decay is dominated by two decay mechanisms. The initial fast discharge is more significant for samples annealed at lower temperatures. The cross-sectional transmission electron microscopic observations show the quasi-continuous Ge layer with Ge nanocrystals and Ge-rich amorphous regions for samples annealed at lower temperatures. Therefore, the fast discharging is attributed to lateral charge loss of insufficiently localized nanocrystals. On the other hand, the slow discharge is attributed to tunneling out of the stored charges in completely localized Ge nanocrystals via the tunneling barrier. © 2003 American Institute of Physics.

The synthesis of Si/Ge nanocrystals has emerged as one of the most attractive scientific research issues after the discovery of light-emitting behavior from porous Si.1 With the hope of the integration of Si-based optoelectronic devices, the various synthesis methods of nanocrystals have been intensively investigated including plasma enhanced chemical vapor deposition (CVD),2 cosputtering,3 low-pressure CVD,4 and ion implantation.5

In addition to the light-emitting property, a nanocrystal in a dielectric matrix has attracted much attention as a promising candidate for a charging node in a single electron memory device (SEMD). Tiwari et al.6 have demonstrated the room-temperature-operating SEMD with Si nanocrystal charging nodes. Their SEMD had a faster writing/erasing time, lower operating voltage, and longer characteristic charge retention time as compared to conventional floating gate memory devices. The charge retention property is inferred from the spatial localization of nanocrystals preventing charge loss via lateral tunneling. Also the thinner tunneling barrier plays an important role in achieving faster writing/erasing. King et al.7 have recently demonstrated the superior properties of Ge-based SEMD over Si-based SEMD in terms of the writing/erasing time and the operating voltage. Despite the promising properties of Ge-based SEMD, most of works concerning charging/discharging behavior have concentrated on the Si-based nanocrystal system.8 Kobayashi et al.9 have reported capacitance–voltage (C–V) hysteresis indicating the charge storage in Ge nanocrystals during C–V sweeping. However, the nanocrystals randomly dispersed in the SiO2 matrix should yield ensemble-averaged information. Specifically, the random distribution would result in the tunneling distance fluctuation and thereby hinder the detailed analysis of tunneling-out mechanism.

Recently, Teo et al.10,11 and our previous report have explored the charge storage effect in Ge nanocrystals.10,11 The nanocrystals were almost arranged in a layer. However, the further investigation of the charge retention property by the capacitance decay in conjunction with various characterizations including C–V measurements and detailed cross-sectional transmission electron microscopic (TEM) analysis is required to clarify the charge retention mechanism.

First, ultrathin SiO2 tunneling layer (~3.5 nm) was formed on p Si (~10 Ω cm as measured by the four-point probe method) by a rapid thermal oxidation process at 1000 °C. An eclipse pulsed laser deposition (PLD) method was used for the growth of thin amorphous Ge (a-Ge) films. Due to a problem of the deposition of clusters and particulates, the eclipse method introduces a shield between the substrate and target to block the clusters and the particulates during deposition. In this case, the method needs an ambient gas as a scattering source during deposition. The working pressure of Ar was 5 mTorr. A commercially available target of a polycrystalline 1 in. Ge pellet was used and a third-harmonic 355 nm Q-switched Nd–YAG laser was used. The energy density was about 1.6 J/cm2. The thickness of the deposited a-Ge layer was 3 nm. Nominally 20 nm thick SiO2 films for gate oxide were deposited by the reactive eclipse PLD method. The Si target was a 1 in. pellet and the pressure of the O2 ambient gas was 6.5 mTorr. The stoichiometry of the SiO2 layer was confirmed by spectroscopic ellipsometry.

The samples were annealed by a rapid thermal annealing (RTA) system with various annealing temperatures from 600 to 850 °C under a N2 ambient for 5 min. After RTA, aluminum as a gate electrode (0.5 mm diameter) was evaporated on the top of the sample using a shadow mask technique. For

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back side contact, an In–Ga eutectic was used after removing oxide on the back side by diluted HF. For $C−V$ measurements of the metal–oxide–semiconductor (MOS) capacitors, a Keithley 590 $C−V$ analyzer (1 MHz) was used. The gate bias sweeping was started from the inversion region (+5 V) after waiting a sufficient period of time for thermal equilibrium (i.e., reverse bias sweeping). Then, the bias was swept back from the accumulation region (−5 V) to the inversion region (i.e., forward bias sweeping). The sweep rate was kept at 2 V/s. For capacitance decay measurements, the samples were initially biased at 5 V for 30 s for electron charging. Then, the bias was rapidly changed to the flat-band voltage. The capacitance decay was recorded for 10 000 s. All measurements were done at room temperature and dark conditions. After the extensive characterizations, the atomic images of nanocrystals were investigated by high-resolution TEM using the same sample.

Figure 1 displays the normalized $C−V$ hysteresis curves with various annealing temperatures. As observed in Fig. 1(a), the $C−V$ hysteresis width increases as the annealing temperatures increase to 700°C. This indicates nanocrystal formation during annealing. The maximum hysteresis width is obtained for the sample annealed at 700°C indicating the maximum nanocrystal density. As annealing temperatures increase further to 850°C as shown in Fig. 1(b), the hysteresis width decreases indicating the decrease of the nanocrystal density by the agglomeration of Ge nanocrystals. As observed in Fig. 1(b), significant $C−V$ stretch out is observed for high-temperature-annealed samples. The result indicates that the diffused Ge generates a large density of interface traps. As reported in the recent TEM investigations, the segregation effect of Ge at the Si/SiO2 interface may deteriorate the $C−V$ characteristics. One interesting observation is made for the sample annealed at 850°C. The $C−V$ hysteresis loop is in the clockwise direction. The hysteresis loop direction is usually counter clockwise as when p Si is used as a substrate. Presumably, the reverse hysteresis effect is due to the additional inclusion of an annealing-induced Ge defect in charging/discharging. The additional possibility of this being due to a small mobile ion density could not be ruled out.

The maximum flat-band voltage shift of 3.8 V is obtained for the sample at 700°C. The stored charge density, $n_{\text{charge}}$, is about $2 \times 10^{12}$ cm$^{-2}$ estimated by using a simple formula given by

$$n_{\text{charge}} = C_{\text{ox}} \Delta V_{FB} / q t_{\text{ratio}},$$

where $C_{\text{ox}}$ is the oxide capacitance and $\Delta V_{FB}$ is the flat-band voltage shift. The factor, $t_{\text{ratio}}$ is the thickness ratio of $t_{\text{gateox}} + 0.5D_{nc}/t_{\text{total}}$ reflecting the effective voltage drop. Here, $t_{\text{gateox}}$, $D_{nc}$, and $t_{\text{total}}$ are the thickness of upper gate oxide, nanocrystal diameter, and total thickness of MOS structure, respectively.

Figure 2 shows the cross-sectional TEM pictures for samples after RTA showing the structural evolution on annealing temperatures. For the sample annealed at 600°C [Fig. 2(a)], the Ge layer is almost continuous. No significant effect of annealing is observed. However, for the sample annealed at 700°C, the undulation of the Ge/SiO2 interface due to the agglomeration of Ge is visible. We observe the fringes showing the crystalline state of Ge. In addition, the amorphous phase between Ge nanocrystals is also discernable by the contrast difference due to the density difference of the

![Figure 1](image1.png)

![Figure 2](image2.png)
material. The amorphous phase may be pure Ge or Ge-rich (Ge+SiO2) mixture. One should note that the annealing condition of 700 °C shows the maximum width in the $C-V$ hysteresis curve. Though nanocrystal density shows the maximum, the layer is still quasi-continuous. Figure 2(c) shows the TEM picture of the sample annealed at 800 °C showing the complete isolation of the Ge nanocrystals. The diameter of the Ge nanocrystals is approximately 5 nm and the shape of Ge nanocrystals is almost spherical.

To elucidate the discharging mechanism of charges in Ge nanocrystals, the capacitance decay is investigated. Figure 3 shows the normalized excess capacitance decays for samples with various annealing temperatures. The normalized excess capacitance, $\Delta C_{\text{excess}}$ is defined as

$$\Delta C_{\text{excess}} = \{C(t) - C_{\text{FB}}\} / \{C(0) - C_{\text{FB}}\},$$

where $C(t)$ is the capacitance at measurement time and $C_{\text{FB}}$ is the flat-band capacitance during forward bias sweeping. The general feature of the decay curves consists of two distinct decay regimes. First, is the initial fast decay and the other is the later slow decay. The initial fast decay is fairly dramatic for the samples annealed at 650 °C. However, there is still remaining excess capacitance even after 10,000 s discharging. The remaining capacitance is about 36% of the initial excess capacitance. Upon increasing the annealing temperatures, the initial fast decay is suppressed. Finally, for samples at 850 °C, the initial decay is virtually absent.

As observed in Fig. 2(b), nanocrystals are not completely localized due to the insufficient annealing temperature and time. Furthermore, the $a$-Ge-rich region, having a much smaller band gap than that of SiO2, exists between Ge nanocrystals. The regions give a lateral channel that allows charge transport along the Ge layer. The inset in Fig. 3 shows a band diagram describing the situation for the lateral charge loss. This effect results in the fast capacitance decay. On the other hand, some of nanocrystals may be well localized by chance. In this case, the only possibility of charge loss is the tunneling out via the tunneling barrier. Thus, the stored charges in the localized nanocrystals will exhibit long-term retention property. This contributes to the slow capacitance decay. Winkler et al. have already observed the capacitance decay with two time scales for MOS with Si nanocrystals. They discussed the initial fast decay as a result of Coulomb repulsion of several electrons in a nanocrystal. However, the fast decay they observed may be due to the lateral charge loss as we discussed in the present study. The transformation technique from the continuous layer to a discrete nanocrystal array via annealing is quite a general approach for SEMD fabrication. King et al. have also employed the RTA technique for nanocrystal isolation. The initial charge loss due to the incomplete isolation could lead to a serious stability problem during device operation. Furthermore, for Ge-based SEMD, the process window for the isolation of nanocrystals would be quite narrow since Ge has a high diffusion coefficient as compared to Si.

To conclude, we have investigated the RTA effect on the charge storage characteristics in MOS capacitors with Ge nanocrystals. The $C-V$ curves showed the hysteresis indicating the charge storage effect in Ge nanocrystals during bias sweeping. The hysteresis width had a strong annealing temperature dependence and showed the maximum at about 700 °C. From capacitance decay experiments at a flat-band voltage, we found that the discharging behavior was dominated by two different mechanisms. The initial fast discharging was more significant for samples annealed at lower temperatures. TEM observation revealed that the Ge layer is quasi-continuous with Ge nanocrystals and $a$-Ge-rich regions. Therefore, the fast discharging was attributed to lateral charge loss of insufficiently localized nanocrystals.

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