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Rapid Thermal Annealing Effect on Charge Storage Characteristics in MOS Capacitor with Ge Nanocrystals

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The rapid thermal annealing effect on charge storage characteristics in metal-oxide-semiconductor (MOS) capacitors with Ge nanocrystals is invesigated by means of capacitance-voltage (*C-V*) and capacitance decay measurements. The *C-V* curves show the hysteresis indicating the charge storage effect in Ge nanocrystals. The hysteresis width shows strong annealing temperature dependence and shows the maximum at 700 °C annealing temperature meaning the optimum annealing condition. From capacitance decay experiment at flat band voltage, we observe initially fast and very slow discharging behaviors. The fast discharge is more significant for samples annealed at lower temperatures. Therefore, the fast discharging is attributed to lateral charge loss of insufficiently localized nanocrystals. The slow discharge is attributed to the stored charges in completely localized Ge nanocrystals.

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I. INTRODUCTION

The synthesis of Si/Ge nanocrystals has emerged as one of the most attractive scientific research issues after the observation of their light emitting behavior [1]. With a hope of the integration of Si-based optoelectronic devices, the various synthesis methods of nanocrystals have been intensively investigated including plasma enhanced chemical vapor deposition (CVD) [2], co-sputtering [3], low pressure CVD [4] and ion implantation [5]. Recent successful results have demonstrated the obvious blue shift of the light emission wavelength of Si nanocrystal due to quantum confinement effect as decreasing its size [4]. Similar behavior has been observed for Ge nanocrystals [6]. The wavelength tuning property of nanocrystals is very promising for Si-based optoelectronic applications.

In addition to their light emitting property, nanocrystals in a dielectric matrix have attracted much attention as a promising candidate for a charging node in a single electron memory device (SEMD) [7]. Tiwari *et al.* have demonstrated the room-temperature-operating SEMD with Si nanocrystal charging nodes. Their SEMD had faster in writing/erasing time, lower operating voltage, and longer characteristic charge retention time as compared to conventional floating gate memory devices [8]. The charge retention property is due to the spatial localization of nanocrystals preventing charge loss via lateral tunneling. Also thinner tunneling barrier plays an important role in achieving faster writing/erasing. King *et al.* have recently demonstrated the superior properties of Ge-based nanocrystal memory device over Si-based nanocrystal memories in terms of the writing/erasing time and the operating voltage [9]. Despite the promising properties of Ge-based nanocrystal memory, most works concerning charging/discharging behavior have concentrated on the Si-based nanocrystal systems [10]. Kobayashi *et al.* have reported *C-V* hysteresis of their metal-insulator-semiconductor (MIS) capacitor indicating the charge storage in Ge nanocrystals during *C-V* sweeping [11]. However, their nanocrystals are randomly dispersed in SiO_2 matrix. Randomly distributed nanocrystals should yield ensemble-averaged information.

Recently we have reported a preliminary result concerning the charging kinetics of metal-oxide-semiconductor (MOS) capacitor with Ge nanocrystals [12]. In the previous investigation, the MOS capacitor was fabricated by rapid thermal oxidation (RTO) for the structure deposited by pulsed laser deposition (PLD). We found some difficulties in analyzing the charging/discharging behaviors of the MOS capacitors due to the remaining polycrystalline silicon layer which is partially oxidized.

In this paper, we sequentially deposite amorphous Ge and SiO_2 layers by reactive PLD. The amorphous

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Ge layer is transformed to nanocrystals arranged in a layer by subsequent rapid thermal annealing (RTA). The charge storage characterisics of the MOS capacitors with various annealing temperatures from 600 °C to 850 °C are investigated.

II. EXPERIMENTAL DETAILS

First, ultra-thin SiO_2 tunneling layer ($\sim$ 3 nm) was formed on p-Si ($\sim$ 10 Ω·cm as measured by four point probe method) by RTO process at 1000 °C employing a custom-built RTO chamber with a bank of tungsten-halogen lamps with the introduction of 5N-grade pure O_2. Prior to the oxidation, the substrate was cleaned by standard RCA steps and remaining oxide was removed by diluted HF. Nominally 3 nm-thick amorphous Ge (a-Ge) layer was deposited by a PLD (third-harmonic 355 nm Q-switched Nd:YAG laser) in Ar ambient ($\sim$ 5 mtorr). 30 nm-thick SiO_2 layer was deposited by a reactive PLD. During SiO_2 deposition, evaporated Si was oxidized under O_2 ambient by reactive process. The stoichiometry of SiO_2 layer was confirmed by spectroscopic ellipsometry measurement. The energy density during PLD was $\sim$ 2 J/cm^2. The pulse repetition rate were 2 Hz for a-Ge growth and 10 Hz for amorphous Si (a-Si) growth, respectively. For these repetition rates, the growth rates were 0.0056 nm/s for a-Ge and 0.016 nm/s for a-Si. A mask is inserted in between target and substrate to avoid the cluster deposition.

The samples were annealed with various annealing temperatures from 600 °C to 850 °C under N_2 ambient. After RTA, aluminum as a gate electrode (0.5 mm diameter) was evaporated on the top of the sample using a shadow mask technique. For back side contact, In-Ge eutectic was used after removing oxide on the back side by diluted HF.

For *C-V* measurements of the MOS capacitors, Keithley 590 *C-V* analyzer (1 MHz) was used. The gate bias sweeping was started from inversion region (+ 5 V) after waiting sufficient time for thermal equilibrium (*i.e.* reverse bias sweeping). Then the bias was swept back from accumulation region (− 5 V) to the inversion region (*i.e.* forward bias sweeping). The sweep rate was kept at 2 V/s. For capacitance decay measurements, the samples were biased at 5 V for 30 s for electron charging. Then the bias was rapidly changed to desired bias. The capacitance decay was recorded for 10,000 s. All measurements were done at room temperature and dark condition.

III. RESULT AND DISCUSSIONS

Figure 1 and 2 display the normalized *C-V* hysteresis curves with various annealing temperatures. As observed in Fig. 1, the *C-V* hysteresis width increases as increasing the annealing temperature to 700 °C. This indicates

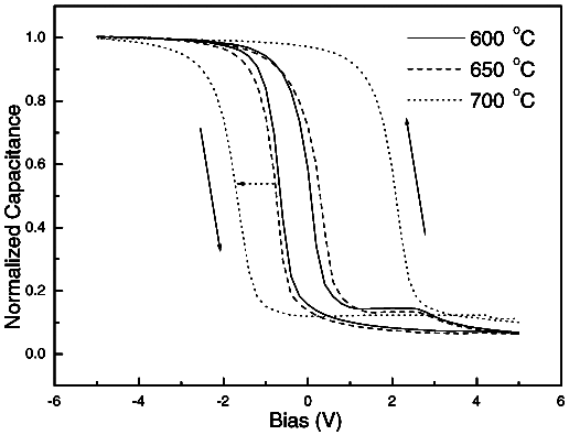

Fig. 1. *C-V* hysteresis curves for MOS capacitors with various annealing temperatures (600 °C, 650 °C, and 700 °C).

nanocrystal formation during the annealing. The maximum hysteresis width is obtained for the sample annealed at 700 °C indicating the optimized nanocrystal formation. As further increasing annealing temperature to 850 °C, the hysteresis width decreases meaning the decrease of the nanocrystal density. The nanocrystal density decreases due to significant Ge diffusion into SiO_2 matrix. Choi *et al.* have observed the optimized annealing temperature at about 750 °C by extensive Raman observations [13]. Our result is in agreement with their result. As observed in Fig. 2, significant *C-V* stretch out is observed for high temperature annealed samples. The result indicates that the diffused Ge generates large density of interface traps. As reported in the recent transmission electron microscope investigations [13], the segregation effect of Ge at the Si/SiO_2 interface may deteriorate the *C-V* characteristics. One interesting observation is made for the sample annealed at 850 °C. The *C-V* hysteresis

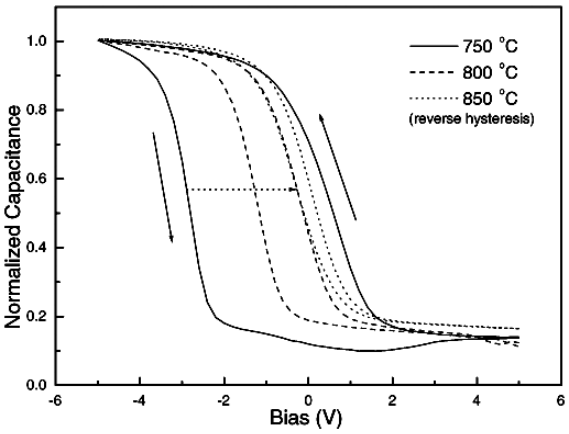

Fig. 2. *C-V* hysteresis curves for MOS capacitors with various annealing temperatures (750 °C, 800 °C, and 850 °C). Reverse hysteresis curve is obtained for 850°C annealing temperature.

loop is clockwise direction. The hysteresis loop direction is usually conter clockwise as far as p-Si is used as a substrate. Presumably, the reverse hysteresis effect is due to some Ge-induced traps. However, the detailed origin is not clear.

Figure 3 shows the flat band voltages as a function of annealing temperature for forward and reverse bias sweepings. The maxium flat band voltage shift of 3.8 V is obtained for the sample at 700 °C. The stored charge density is about 2.5 $\times$ 10^{12} cm^{-2} estimated by using a simple formular of $(C_{ox}/q)\Delta V_{FB}$, where C_{ox} is the oxide capacitance and ΔV_{FB} is the flat band voltage shift. The density could be underestimated because our voltage sweeping rate is relatively fast.

To eluciate the discharging mechanism of charges in Ge nanocrystals, the capacitance decay is investigated. Figure 4 shows the normalized excess capacitance decays for samples with various annealing temperatures. The excess capacitance, ΔC_{nom} is defined as;

$$\Delta C_{nom} = (C(t) - C_{FB})/(C(0) - C_{FB}) \quad (1)$$

where $C(t)$ is the capacitance at measurement time and C_{FB} is the flat band capacitance during forward bias sweeping.

The rapid capacitance decay is observed for the samples annealed at 650 °C. However, there is still remaining excess capacitance even after 10,000 s discharging. The remaining capacitance is about 0.36 of the initial excess capacitance. Therefore, the capacitance decay behavior shows two different discharging mechanisms. Due to the insufficient annealing temperature, nanocrystals are not completely localized. Then significant charge loss may occur laterally. This effect results in the fast capacitance decay. However, some of nanocrystals are well localized. The stored charges in the localized nanocrystals will exhibit long retention times. As increasing annealing temperatures, the localization of nanocrystals is accelerated. Therefore, the initial fast capacitance decay is strongly suppressed. Though the density of nanocrystals is quite low for samples annealed at 850 °C, the fast capacitance decay is virtually absent.

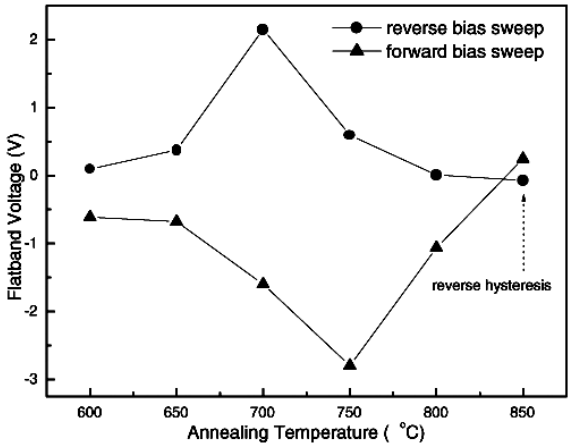

Fig. 3. Flat band volatage vs. annealing temperature for forward and reverse bias sweepings. Note that flat band voltage for forward bias sweeping is larger than that for reverse bias sweeping for 850 °C annealed sample. This is due to the reverse hysteresis.

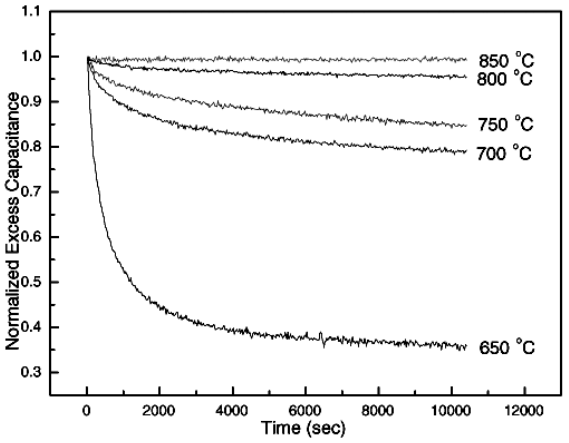

Fig. 4. Normalized excess capacitance decays for samples with various annealing temperatures.

IV. CONCLUSION

We have investigate the rapid thermal annealing effect on charge storage characteristics in MOS capacitors with Ge nanocrystals by means of capacitance-voltage (C-V) and capacitance decay measurements. The C-V curves showed the hysteresis indicating the charge storage effect in Ge nanocrystals during bias sweeping. The hysteresis width exhibited strong annealing temperature dependence and showed the maximum at about 700 °C annealing temperature. The maximum flat band voltage shift was about 3.8 V and the estimated stored charge density was about 2.5 $\times$ 10^{12} cm^{-2}. From capacitance decay experiment at flat band voltage, we found discharging behavior was governed by two different mechanisms. The fast discharging was more significant for samples annealed at lower temperatures. Therefore, the fast discharging was attributed to lateral charge loss of insufficiently localized nanocrystals. In contrast, remaining capacitance with long retention time may be due to the charges in completely localized Ge nanocrystals. The present investigation demonstrates that RTA is feasible for controlling both the nanocrystal density and the retention time.

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