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Novel growth and properties of GaAs nanowires on Si substrates

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Abstract
Straight, vertically aligned GaAs nanowires were grown on Si(111) substrates coated with thin GaAs buffer layers. We find that the V/III precursor ratio and growth temperature are crucial factors influencing the morphology and quality of buffer layers. A double layer structure, consisting of a thin initial layer grown at low V/III ratio and low temperature followed by a layer grown at high V/III ratio and high temperature, is crucial for achieving straight, vertically aligned GaAs nanowires on Si(111) substrates. An in situ annealing step at high temperature after buffer layer growth improves the surface and structural properties of the buffer layer, which further improves the morphology of the GaAs nanowire growth. Through such optimizations we show that vertically aligned GaAs nanowires can be fabricated on Si(111) substrates and achieve the same structural and optical properties as GaAs nanowires grown directly on GaAs(111)B substrates.

1. Introduction
Recently, semiconductor nanowires (NWs) have been in the spotlight as nano-building blocks for future integrated electronic and optoelectronic devices. III–V compound semiconductor NWs have the potential to be grown epitaxially on Si substrates, which would then allow the integration of III–V–based optoelectronics with established Si microelectronics technologies [1–3]. Achieving this integration, however, requires overcoming a number of specific problems caused when two dissimilar materials from group IV and III–V form a heterostructure interface [4, 5]. These problems include lattice and thermal expansion mismatch, and the formation of anti-phase domains [6–8]. For the case of Si in particular, the existence of a native oxide layer on the surface is a major factor preventing the epitaxial growth of III–V NWs [1]. Therefore, overcoming these interface issues—lattice mismatch, different thermal expansion coefficients, and the interruption from native oxide layers—is a crucial factor for obtaining high quality III–V NWs on Si substrates.

As recently demonstrated by Bao et al [9], GaAs NWs can be epitaxially grown on Si(111) substrates by metal-organic vapor phase epitaxy (MOVPE) via the vapor–liquid–solid (VLS) mechanism. In their work, careful control over the NW nucleation stage using substrate etching and preparation, baking process, and specific growth temperature was found to be crucial. However, there are only few reports of epitaxial growth of vertically straight III–V NWs on Si substrates which...
have been published [1, 9, 10], possibly due to the difficulty in controlling the surface properties of Si. A simpler and easily reproducible approach is highly desirable to achieve vertically straight (epitaxial) III–V NWs on Si.

In this paper, epitaxial growth of high quality vertical GaAs NWs on Si(111) substrates was achieved. Prior to initiating GaAs NW growth, thin GaAs buffer layers were deposited on the Si substrates. Since the initial nucleation of the NWs is very dependent on the quality of the surface, achieving buffer layers with good morphology and crystallinity is important [11]. In the last 2 decades or so, much effort has been devoted to the growth of III–V semiconductor epilayers on Si. It has been found that III–V semiconductor layers grown on Si substrates with high V/III flow ratio at high temperature have good crystal structure [12, 13] but rather than forming a continuous layer, growing into island structures due to the strain effect resulting from lattice mismatch (4% of GaAs/Si) and different interface energy [14, 15]. The layer is approximately 1 μm thick before the islands coalesce to form a continuous layer, but by then other undesirable effects (such as lattice relaxation, anti-phase domain formation) become an issue [16, 17]. The layers grown with low V/III ratio at low temperature, in contrast, are able to form thin continuous layers. However, the quality of the layers is relatively low with significant carbon contamination [13]. In this work, a buffer layer must satisfy at least two requirements: it must cover the whole surface as a continuous layer and have good surface and structural quality for the nucleation of NWs. To achieve this, we grew buffer layers in a two-step process. First, an initial GaAs layer was grown on Si substrates with low V/III ratio at low temperature. Then a subsequent GaAs layer was deposited with high V/III ratio at high temperature. By using this two-step procedure, high quality buffer layers of only a few tens of nanometers thick have been achieved. We refer to this structure as the ‘double buffer layer’ structure.

Annealing at high temperature is a common process used to recover structural quality in materials. In the highly damaged semiconductor materials, for instance, by ion bombardment, the high temperature annealing allows atoms to move back into their lattice sites, removing structural damage and recrystallize material from an amorphous structure to a crystalline or polycrystalline structure [18]. Annealing after buffer layer deposition can improve the quality of the buffer layers [17] as well as the surface smoothness. This could potentially improve catalyst (Au) attachment and the nucleation of NWs. Accordingly, an in situ high temperature annealing was performed for some double buffer layer structures.

2. Experimental details

GaAs NWs were grown using Au catalyst via VLS mechanism on the Si(111) substrates with and without GaAs buffer layers, and directly on GaAs(111)B (as-terminated surface) substrates for comparison. Both GaAs layers and NWs were grown by horizontal flow low pressure MOVPE at 100 mbar. Trimethylgallium (TMGa) and arsine (AsH₃) were used as group III- and V-source materials, respectively.

2.1. Sample preparation

Si substrates were [111] oriented with 4° mis-cut toward the [112] direction. In order to remove organic contaminants, the substrate was cleaned by dipping in trichloroethylene (TCE) solution, then acetone and followed by methanol for 5 min each and then rinsed with de-ionized water. A 5 min diluted HF (4.8%) etch was used to remove the native oxide from the Si surface. The substrate was immediately transferred into the MOVPE reactor within 10 s after etching to prevent regrowth of native oxide layer. The substrates were pre-annealed at 750°C under H₂ atmosphere for 10 min to remove remaining contaminants and then under AsH₃ for 10 min to create an As-rich surface.

2.2. Buffer layer growth

For single buffer layer structure, only one GaAs layer was grown on Si substrates at 400°C for 60 min with V/III ratio of 15.4. The V/III growth ratio was controlled by flow rates of TMGa (5.785 × 10⁻⁵ mol min⁻¹) and AsH₃ (8.929 × 10⁻¹ mol min⁻¹). This single buffer layer also acts as the initial layer in the double buffer layer structure, where the subsequent GaAs buffer layer was grown at 700°C for 10 min with a V/III ratio of 154.3 (TMGa: 1.157 × 10⁻⁵ mol min⁻¹ and AsH₃: 1.786 × 10⁻³ mol min⁻¹). There was no growth interruption during the heating up step from 400 to 700°C. After the deposition of the subsequent GaAs buffer layer, several samples were annealed in situ at 750°C for 15 min under AsH₃ atmosphere where the AsH₃ atmosphere prevents desorption of As from the GaAs buffer layers.

2.3. GaAs nanowire growth

These Si substrates coated with single or double GaAs buffer layers, together with untreated Si(111) and GaAs(111)B substrates were then functionalized by immersion in poly-L-lysine (PLL) solution for 1 min. This PLL treatment gives the surface a positive charge to attach the negatively charged colloidal Au nanoparticles. After rinsing in DI water, a droplet of Au colloidal solution containing Au particles of 50 nm in average diameter (4.5 × 10¹⁰ nanoparticles ml⁻¹) was applied and then rinsed with DI water. The wafers were then loaded into the reactor and annealed under AsH₃ ambient at 650°C for 10 min before NW growth. GaAs NWs were grown at 450°C for 30 min with V/III ratio of 46.3 (TMGa: 1.157 × 10⁻⁵ mol min⁻¹ and AsH₃: 5.357 × 10⁻⁴ mol min⁻¹). For PL measurements an AlGaAs shell was grown over the GaAs NWs to passivate the GaAs surface [19, 20]. The AlGaAs shell growth was performed at 650°C for 20 min with an Al vapor concentration of 26% and the same flows of TMGa and AsH₃ as described above. Finally, in order to prevent oxidation of AlGaAs shell from exposure to air, a thin GaAs cap layer was grown at 650°C for 5 min with V/III ratio of 33 (TMGa: 1.620 × 10⁻³ and AsH₃: 5.357 × 10⁻⁴ mol min⁻¹).

2.4. Buffer layer and nanowire characterization

The GaAs buffer layers and NWs were characterized by field-emission scanning electron microscopy (SEM), transmission
Figure 1. Schematics of the Si substrates coated with (a) single buffer layer, (b) double buffer layers, and (c) annealed double buffer layers; (d)–(f): SEM images for the surface morphology of single buffer layer, double buffer layers, and annealed double buffer layers, respectively; high resolution (HR) cross-sectional TEM images for (g) single buffer layer, (h) double buffer layers, and (i) annealed double buffer layers (S: Si substrate, L\textsubscript{I}: The initial/single GaAs buffer layer and L\textsubscript{S}: The subsequent GaAs buffer layer, G*: Amorphous glue used during sample preparation).

Results and discussion

The schematics of the three different types of GaAs buffer layers are shown in figures 1(a)–(c). First, the single buffer layer (figure 1(a)) grown on Si(111) substrates at low temperature (400°C) with low V/III ratio (15.4) has a rough surface as seen in the SEM image (figure 1(d)). We speculate that during growth, island formation initially takes place due to the thermal and lattice mismatch between the Si substrate and the growing GaAs material [14, 15] until finally the layer forms a polycrystalline structure made up of the coalescence of these small islands. A high resolution TEM (HR-TEM) image of the single buffer layer (figure 1(g)) illustrates that abundant structural defects exist in this thin buffer layer (∼12 nm), such as dislocations and stacking faults, with surface irregularity. The poor crystalline quality of this single buffer layer indicates that it is not suitable for the subsequent growth of NWs (discussed later).

Figure 1(e) is the SEM image taken from the double GaAs buffer layer structure and shows the surface with triangular terraces and the occasional presence of voids. The triangular symmetry of the crystals is related to the zinc-blende (ZB) structure of GaAs grown on a (111) surface. The upper surfaces of the terraces are GaAs(111) surfaces tilted from the substrate, which is consistent with the 4° mis-cut of the Si substrate. The TEM image (figure 1(h)) taken from the [110] zone axis shows that the upper region of the GaAs layer is almost free of lattice defects and superior to the single buffer layer.

In situ annealing effectively improves the surface morphology of the double buffer layer structure as seen in SEM image (figure 1(f)). The triangular terraces have become smoother and the surface voids have also disappeared due to recrystallization. TEM image (figure 1(i)) shows that the subsequent GaAs layer is still free of lattice defects and the lattice faults in the initial layer are also reduced after annealing.

In figure 2, the XRD reciprocal space map taken from [111] symmetric reflection shows that the substrate peak (S) and the buffer layer peak (L) are separated along the Ω/2θ axis. The separation is almost consistent with the lattice mismatch (∼4%) between GaAs and Si(111), indicating that the GaAs buffer layer is fully relaxed. More importantly, both peaks lie along the same Ω with close d-spacing, an indication that the
buffer layers have the same crystal structure and bear a close epitaxial relationship to the Si substrate. SEM images in figure 3 show the morphology of the GaAs NWs grown on the Si(111) substrates directly and coated with various GaAs buffer layers. In all cases except the direct growth of GaAs NWs on Si substrates, most GaAs NWs grow vertically along the [111] direction, indicating the epitaxial relationship of NWs with the buffer layers and substrates. The average length and density of NWs from these samples are summarized in table 1.

Figure 3(a) shows a typical SEM image of GaAs NWs grown directly on Si(111) substrate, where very low density (~0.04 μm⁻²) of NWs were observed and exhibit a random growth direction (~10% of the NWs are vertical). Although HF etching was used to remove the native oxide on the Si surface prior to the application of Au particles, it was likely that surface oxidation reoccurred during the DI water rinsing step. This oxide layer most likely resulted in lower adhesion of the Au particles despite the use of PLL. However, images of figures 3(b)–(d) clearly show that GaAs buffer layers can dramatically improve the morphology of GaAs NWs. In the case of single GaAs buffer layer (figure 3(b)), the density of NWs was improved by ~5 times though it is still rather low—only ~0.25 μm⁻². In addition, the NWs have a large variation in the length distribution and the yield of straight NWs is only ~75% as listed in table 1. Since the initial nucleation step of NW growth determines the NW growth direction [9, 21], the rough surface and irregularity of the single buffer layer resulted in kinked or non-vertical NWs. Also, the poor surface of the single GaAs buffer layer results in an irregular length distribution of the NWs. NWs grown on double GaAs buffer layers have much improved morphology with only a small fraction of kinked NWs as shown in figure 3(c). The density and the yield of the vertical NWs have increased significantly and the length distribution of the NWs is more uniform than that grown on single buffer layers. Due to the improvement of surface smoothness and reduction in surface irregularity there is a higher density of Au particles attached to the double buffer layers than to the single buffer layer as shown in table 1, which accounts for the higher density of NWs grown on the double buffer layers. Better results from the double buffer layer structure than from the single one are attributed to two facts: first, the double layer has less defects and second, the surface appears smoother. They might look rough with a number of terraces but there are large flat surfaces (in figure 1(e)) as opposed to the single buffer layer (small, grainy islands). The morphology of the GaAs NWs is further improved on the annealed double buffer layers. As shown in figure 3(d), nearly all GaAs NWs are
vertical along the [111] direction. The length distribution and yield of vertical NWs are also further improved whilst high density of the NWs (∼0.52 μm⁻²) is achieved. This further improvement is attributed to the high temperature annealing step which could remove the dangling bonds, occasional voids, and rough terrace edges [14]. Although the length of GaAs NWs grown on the double buffer layers on Si wafer is slightly longer than that grown on GaAs(111)B substrates (figure 3(e)), they are almost the same in terms of NW morphology and density. The difference in length may be due to the different surface conditions between the GaAs buffer layers (grown on Si substrates) and the GaAs substrates. It is worth noting that although PLL was used to increase adhesion of Au to the surface for all samples, a substantial drop in the density of NWs was observed in comparison to the Au density. One possibility is the agglomeration by diffusion/Oswald ripening process [22]. However, more experiments are required to clarify this issue.

NW properties depend strongly on growth temperature, V/III flow ratio, and precursor flow rate [1, 3, 9, 23, 24]. In this study, all NWs grown on different buffer layers had almost identical structural and crystallographic properties because the growth parameters were the same. Figure 4 shows the morphology and crystal structure of the GaAs NWs grown on the Si substrates coated with the annealed double buffer layers.

In figure 4(a), the NWs show a tapered shape but they are straight with 4° off the substrate normal, corresponding to the mis-cut angle of the substrate. The tapering parameter is ∼26.67 (nm μm⁻¹), calculated as the change in diameter per unit of NW length (ΔD/ΔL). The cross-section of the NWs has distinctly truncated triangle shape [hexagonal shape having the sides in two different lengths] as shown in figure 4(b) similar to our previously reported GaAs NWs grown on GaAs substrates [25]. Along the length of NWs, rotations (figure 4(b)) and grooves (figure 4(c)) were observed due to the formation of stacking faults [26].

TEM image in figure 4(d) illustrates the overall shape of a single GaAs NW. While the bottom part of NWs (figure 4(e)) shows stacking faults with a saw-teeth shape. Figure 4(f) (inset), however, shows perfect ZB structure with the near-hemispherical Au catalyst on tip of the NW. Figure 4(g) is a high resolution TEM image and shows clearly the ZB structured NW with a thin twin slice (Type A–B–A). In fact, this type of twin defects is commonly associated with the side faceting behavior of ZB III–V NWs [25, 27, 28]. Faceting usually takes place in association with the high density of twins and the saw-teeth faceted sidewalls at high growth temperature [26, 27]. Overall, the structural properties of the GaAs NWs grown on Si wafers with buffer layers are almost same with those of GaAs NWs grown on the GaAs substrates [25, 26].

The optical properties of the GaAs NWs were investigated through micro-PL measurement at low temperature. Figure 5 shows the normalized PL spectra from three single NWs grown...
on the annealed double buffer layers and two single NWs grown on GaAs substrate for comparison. All NWs exhibit nearly identical PL peaks at 1.516 eV, attributed to free exciton recombination. The PL linewidths are similar for all samples, indicating this novel growth approach of GaAs NWs on Si is a very promising way to integrate III–V NW devices onto a Si platform.

4. Conclusions

GaAs NWs were grown on the Si(111) substrates coated with GaAs buffer layers. These buffer layers enable the growth of straight, vertically aligned epitaxial GaAs NWs along (111) direction. A double layer structure consisting of an initial layer grown at low temperature with low V/III flow ratio and a subsequent layer grown at high temperature with high V/III flow ratio results in flat surface and good crystalline quality. In situ annealing at high temperature further improved the surface morphology of the double buffer layers, and subsequently the yield of high quality NWs. GaAs NWs grown on the annealed double buffer layers and directly on GaAs substrates had similar structural and optical properties such as morphology, density, PL emission wavelength and linewidth. These results indicate that the double buffer layer structure is a very attractive alternative to grow high quality III–V NWs for integration of III–V devices with Si-based electronics.

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References


Figure 5. Normalized micro-PL spectra for a single NW grown on Si substrate coated with annealed double buffer layers (red-solid line), and GaAs substrate (black-dotted line).