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Electrical and Structural Properties of Si Nanocrystals Prepared by Ion-Beam-Assisted Electron Beam Deposition

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We fabricate metal-oxide semiconductor (MOS) structures containing Si nanocrystals. The oxide layers are formed by rapid thermal oxidation (RTO) process of amorphous silicon films prepared by electron beam deposition with/without ion-beam-assistance. We observe a singnificant effect of ion-beam irradiation on nanocrystal formation. The transmission electron microscope (TEM) image of the oxide layer deposited by ion-beam-assisted electron beam deposition (IBAED) shows that Si nanocrystals form a band due to their large density near the Si/SiO_x interface. However, No nanocrystal is observed in the TEM image of the sample deposited by electron beam deposition method (EBD). Such a difference manifests that ion-beam-assistance play an important role in the enhancement of nucleation rate. In additon, such a nanocrystal band structure results in an ultra-large capacitance-voltage (C-V) hysteresis. The width of C-V hysteresis for IBAED sample is about 22V, whereas the C-V hysteresis width of EBD sample is less than 1V. Furthermore IBAED sample shows an interesting capacitance transient behavior indicative of non-dispersive carrier relaxation. The charge retention times strongly depend on applied bias and show the maximum of 72 sec near mid-gap voltage. The retention time behavior and large C-V hysteresis suggest that the tunneling of trapped charges in nanocrystals through empty interface states is the main pathway for the charge-loss mechanism.

I. INTRODUCTION

Si nanocrystals have recently attracted much attention because of their light-emitting ability. The light-emitting ability may offer a new class of materials applicable to Si-based optoelectronics [1]. Together with the light emitting property, nanocrystal could be one of good candidates for a memory node in single electron memory device (SEMD). Specifically nanocrystal in a SiO_2 matrix is very attractive. Large band gap and large resistivity of SiO_2 usually ensures the suppression of co-tunneling phenomenon. Furthermore, small nanocrystal has a sufficient charging energy for room temperature operation. [2] Recently Tiwari *et al.* [3] demonstrated room temperature operating SEMD employing nanocrystals. However, random distribution and size fluctuation of nanocrystals are remaining hurdle preventing further progress of nanocrystal-involved devices.

Nanocrystals have been synthesized by several methods including ion implantation [4], co-sputtering [5], and silicon-rich-oxide (SRO) [6], *etc.* However, further research toward the establishment of stable and reliable method compatible with standard CMOS process is required. In this paper, we investigate new method for nanocrystal formation employing Ar ion beam activation during amorphous Si deposition.

II. EXPERIMENTAL DETAILS

Amorphous Si films, 200 nm thick, were deposited either by ion-beam-assisted electron beam deposition (IBAED) or simply electron beam deposition (EBD). Sample surfaces were pre-sputtered to remove native oxide and other contaminants. Then, for IBAED sample, the surface was irradiated by an Ar ion-beam by utilizing a 2-grid Kaufman ion source (Oxford Applied Research MPD22I) during deposition. Ion acceleration voltage was 500 V. For metal-oxide-semiconductor (MOS) structure, some samples are oxidized by employing a custom-built rapid thermal processing system with the introduction of 5N-grade pure O_2 during rapid thermal oxidation

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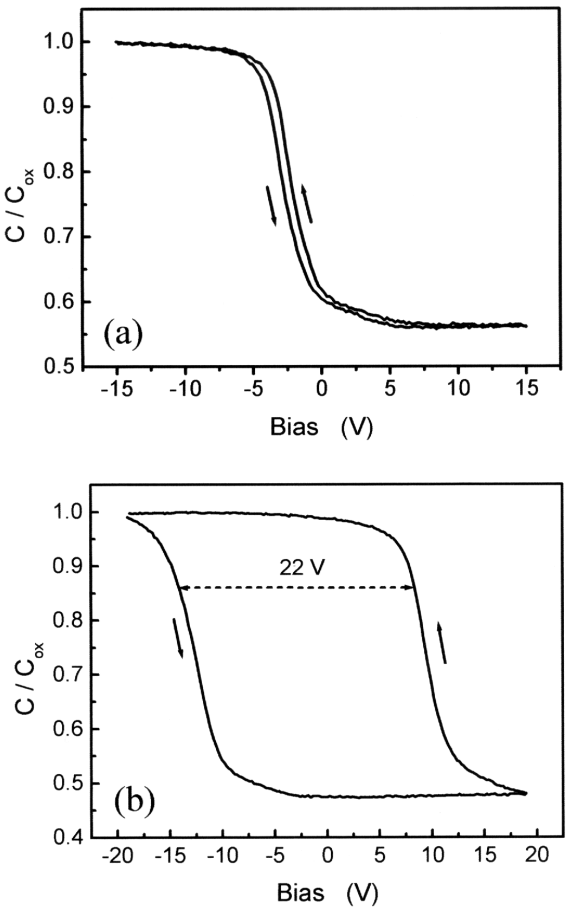

Fig. 1. *C-V* characteristics of EBD sample (a) and IBAED sample (b). A dual sweeping mode is employed for *C-V* characteristics. Arrows in the figures are sweeping directions. Sweeping rate is 2 V/s.

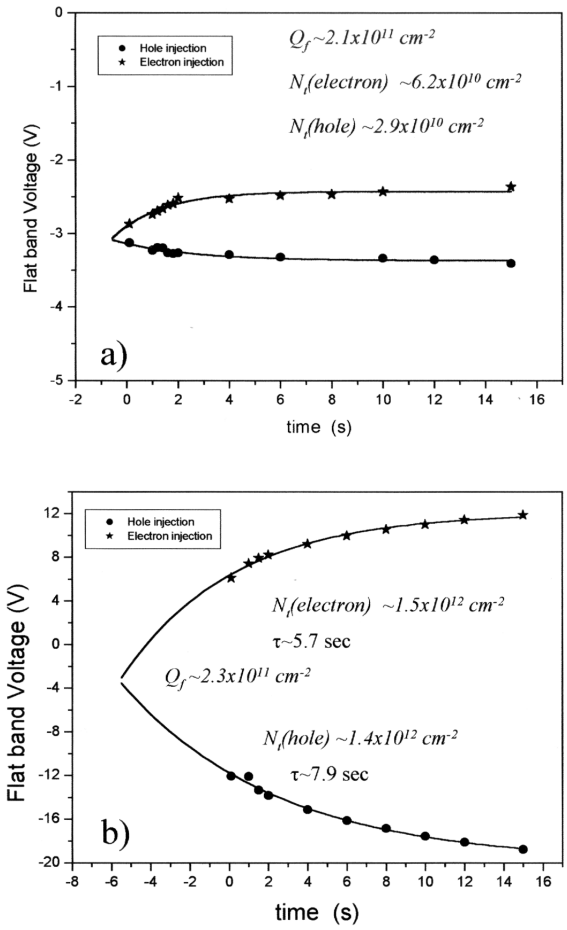

Fig. 2. Flat band voltage shift as a function of injection time of EBD sample (a) and IBAED sample (b). Electrons/holes are injected at +20V/-20V and sweeping rate during measurement is 20 V/s.

(RTO). The flow rate of O_2 was 500 sccm and oxidation temperature was kept at 1000 °C with the typical ramp rate of 100 °C/sec. The oxidation experiments were conducted by using a multiple heating/cooling process to avoid overheating of our system. Each heating time was 150 sec and total heating time was 4500 sec. As a control sample, a piece of p-Si wafer was placed near IBAED and EBD samples. After oxidation, Au dots (1 mm diameter) was evaporated using a shadow mask technique. For back side contact, In-Ga eutectic was used after scratching the surface.

For capacitance-voltage (*C-V*) and capacitance-time (*C-t*) measurements, a Keithley 590 *C-V* analyzer was used. All measurements were done at room temperature. After the extensive characterizations, the atomic images of nanocrystals were investigated by high resolution transmission electron microscopy (TEM).

III. RESULTS AND DISCUSSION

Metal-insulator-semiconductor (MIS) structure employing amorphous Si layer as an insulating layer was leaky and unstable. The structure is not suitable for present charging study. Thus metal-oxide-semiconductor (MOS) structures are fabricated using RTO. For control samples, we observe conventional *C-V* profiles of MOS diode without any hysteresis. As shown in Fig. 1(a), some hysteresis is found for EBD sample. The hysteresis width at flat band voltage is approximately 0.7 V indicative of some charging effect presumably due to some traps with low density. In contrast, for IBAED sample, we observe an ultra-large hysteresis in *C-V* profiles as shown in Fig. 1(b). The width of the hysteresis is over 20 V with 2 V/s sweeping rate. The hysteresis loop direction is counter clockwise. After injecting electrons/holes at 20V (*i.e.* inversion)/-20V (*i.e.* accumulation) upto 15 sec, *C-V* profiles are obtained with fast sweep rate (10 V/s). As shown in Fig. 2(a) and (b), *C-V* profiles show systematic flat band voltage shifts as increasing injection times. The data are fitted with a simple exponential charging model. As observed in the figures, the

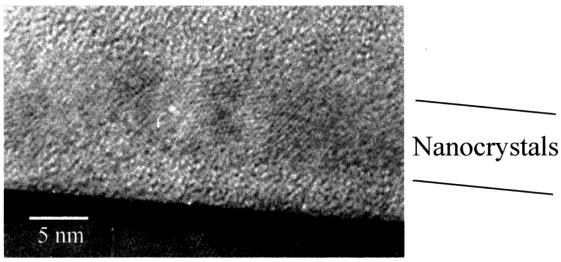

Fig. 3. Cross-sectional TEM image of IBAED sample RTO-treated at 1000 °C.

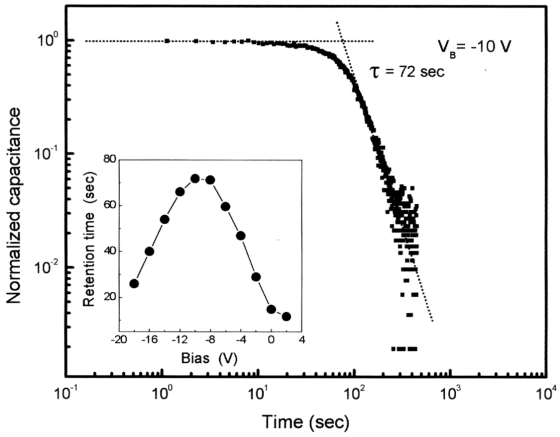

Fig. 4. *C-t* characteristics of IBAED sample at -10 V after injecting electrons at 20 V for 8 sec. The inset shows the retention time variation as a function of bias voltage.

fittings are very successful. The fitting procedure allows us to extract important parameters. For EBD sample, flat band voltage shift is not symmetrical. The density of fixed oxide charges is about 2.1 × 10^{11} cm^{-2}. The saturated density of trapped electrons is about 6.2 × 10^{10} cm^{-2} and the saturated density of trapped holes is about 2.9 × 10^{10} cm^{-2}. For IBAED sample, the density of fixed oxide charges is about 2.3 × 10^{11} cm^{-2}. Suprisingly, the flat band voltage shift is almost symmetrical and thereby the saturated density of trapped carriers is almost the same ($\sim$ 1.4 × 10^{12} cm^{-2}). The result strongly suggest that nanocrystals can capture electrons and holes depending on biasing conditions and the nanocrystal density would be 1.4 × 10^{12} cm^{-2}. The *C-V* hysteresis in the MOS structure has been usually attributed to slow traps or border traps. The border traps are located with a few nm from SiO_2/Si interface. Thus they can communicate with Si substrate by a tunneling process. The hysteresis occurs because the gate bias at which electrons fill the traps is different from the point at which the electrons leave the trap and/or due to the difference between the capture and emssion times of the border traps. Our *C-V* hysteresis of IBAED sample is similar to border-trap-related *C-V* hysteresis. However, border traps are usually generated by X-ray irradiation, avalanche injection, and high field stressing. Our sample preparation condition is far from these conditions. Thus we believe nanocrystals or at least nanocrystal-related traps are responsible for such a large *C-V* hysteresis. This is confirmed by TEM observations. Figure 3 shows the TEM image of IBAED sample. Nanocrystals are concentrated in the localized region close to Si/SiO_x interface. Nanocrystals almost appear as a band due to their large density. The average separation from interface is about 4 nm. For EBD sample, no nanocrystal is found in TEM image.

Ion-beam-assistance during deposition should activate adatom migration and thereby enhance nucleation rate (or structural relaxtion for short range ordering). [8] The nuclei would grow to nanocrystals during subsequent annealing. RTO process of amorphous Si is complicated process because solid phase crystallization in bulk and amorphization by oxidation from surface take place at the same time. The reason why nanocrystal are localized in a narrow region at a certain depth from the Si/SiO_x interface may be a matter of debate. Similar narrow nanocrystal band produced non-intentionally was reported. Such a self-organization of nanocrystals was attributed to collision mixing and near interface oxygen diffusion during ion implantation (75 KeV). [9] Those effects create many nucleation sites near the interface. The self-organized band presented in this work may have a different origin since the accelerationg voltage in our experiments is much lower. We do not have comprehensive model at present. However, one may note the compressive strain present near the interface due to a density mismatch. The strain is relieved by nanocrystal formation at the transition layer. Thus, near the transition border ($\simeq$ 4 nm), the nuclei will have better chance to grow bigger nanocrystals and the bigger crystals will survive during RTO process.

To further elucidate the charging mechanism, *C-t* measurements were carried out varying biasing condition. After injecting electrons at 20 V for 8sec, gate voltage is suddenly changed to measurement voltage. As observed in Fig. 4, discharging occurs drastically and the distinction between "charged states" and "uncharged states" is very clear. Such a distinction allows us to evaluate the charge retention time. The evaluated retention time is about 72 sec at the measurement voltage of -10 V. Tsybeskov *et al.* [10] reported similar *C-t* result in their nanocrystal superlattice structure. They discussed their *C-t* result as indicating non-dispersive carrier relaxation. Similar discussion was made by Maeda *et al.* [11] in describing tunneling current transient of their MOS diode. However, their structures are well designed for having very narrow nanocrystal size distribution with an aid of sophisticated process steps. Thus the non-dispersive carrier relaxation in their reports is not surprising. However, in our IBAED sample, non-intentional design is made in the sense of tunneling barrier thickness and nanocystal size dispersion. Thus our method is attrac-

tive by its simplicity. One more interesting observation is about the bias dependence of charge retention behavior (the inset in Fig. 4). The longest retention time is obtained at the biasing condition near midgap voltage. Shi *et al.* [12] suggested a model to explain the charge storage characteristics in nanocrystals. According to their model, charges were stored at the deep traps of nanocrystals. The dominant charge-loss process was the direct tunneling of the trapped charges to the interface states. Thus the density of the interface states controls the charge-loss rate. Our result could be explained based on Shi's model. At the midgap voltage, charge tunneling mainly occurs to the interface states near midgap where the density of interface states is lowest. Therefore, the longest retention time will be resulted (*i.e.* slowest tunneling out of stored charges).

IV. CONCLUSION

To conclude, we have observed an ultra-large *C-V* hysteresis for a MOS structure containing nanocrystals where the oxide layer was produced by RTO process of amorphous Si deposited by IBAED. From a series of carrier injection experiments at accumulation and inversion bias conditions by varying injection times, the density of nanocrystal-related traps was about 1.4×10^{12} cm^{-2} and the traps can capture electrons and holes. Thus the result provides an evidence that the charging mechanism in nanocrystals is trap-related. Cross-sectional TEM observation confirmed the existence of nanocrystals and the nanocrystals have localized in a narrow region at a certain depth from the Si/SiO$_x$ interface. The localization in the narrow region resulted in a characteristic discharging behavior in *C-t* measurement indicating that the carrier relaxation is non-dispersive. Based on the retention time estimation from *C-t* measurements, it was concluded that the tunneling out of trapped charges in the deep traps of nanocrystals play a role in the charge-loss mechanism.

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